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創傑科技股份有限公司
ISSC Technologies Corp.

Datasheet of Bluetooth

BM77SPP03MC2 Module

ISSC Technologies Corp.

Revision History

Date	Revision Content	Version
2012/10/31	Modified the Calibration values of LDO18	0.3
2013/01/30	Modified Figure Error in page_15	0.4
2013/04/23	Modification of wording. typo correction and the tolerance in Dimension	1.0
2013/06/28	Update the highest baud rate support	1.1
2013/07/09	Add descriptions in current consumption part and update suggested load board foot print information	1.2
2013/08/20	Update UART Baud rate information	1.3
2013/10/01	Update current consumption & Timing Sequence photo	1.4

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Content

1. Introduction

Part Name: ISSC BM77SPP03MC2 Bluetooth module

Part Number: BM77SPP03MC2-xxxxxx

The ISSC BM77SPP03MC2 Bluetooth module is design for Bluetooth standard SPP/ BLE electronic accessories via Bluetooth connectivity. It is available in the 2.4GHz ISM band Class 2 Radio, compatible with Bluetooth Core Specification Version 3.0/ 4.0 + EDR.

ISSC IS1677NM single chip solution combines transceiver and baseband function to decrease the external components. It narrows down the module size and minimizes its cost.

The optimized power design minimize power consumption to keep low battery

1.1. Major Components

- ISSC IS1677NM (40 pin QFN, single-chip Bluetooth transceiver and baseband processor)
- Serial EEPROM 8K (1024*8) TSSOP 8P

1.2. Features

- Bluetooth 3.0/ 4.0+ EDR compliant
- Low power 1.8V RF operation
- RF transmitter output power Class 2
- RF receiver GFSK typical -90dBm, π/4 PSK typical -90dBm, 8DPSK typical -83dBm, BLE typical -92dBm
- Internal ROM and 4Mibts of flash
- I2C for external EEPROM
- 1 LED driver

1.3. Application

- GPS
- Printers
- Electric Scale
- Blood Pressure Monitors
- Bar code Scanner
- Industrial Applications (CNC, PLC, RFID)
- Embedded systems

2. Product Specification

2.1. Chipset

6x6 mm^2 40 pin QFN IS1677NM

2.2. Interfaces

- Multi function GPIO interface
- Bluetooth RF interface
- UART up to 921600 bps
- I2C for external EEPROM

2.3. Hardware Design Considerations

- Power

The module requires either a 4.2- 3.3V

- Power ramp-up timing restriction

1) BAT_IN : ramp-up (0 to 1.6V) < 200ms
2) PMULDO_O : PMU-logic ramp-up (0 to 1.6V) <60ms
3) VCC_RF (1.8V power domain) : RF BPOR ramp-up (0 to 1.6V) < 20ms

- Power on sequence

1) BAT_IN: must be first!
2) 3.3V power domain: VDD_IO/ VDD_FIO must power-up early than 1.8V power.
3) 1.8V power domain: 1V8/ VCC_RF/ VDD_XO/ 1V8_U_P
4) RST_N: digital reset released from 0 to 1.6V must be the last one.

- Recommended operating conditions

Rating	Min	Typ	Max
VDD_IO_x,	3.1V		3.63V
SW_BTN	3.2V		4.3V
BAT_IN	3.2V		4.3V

- Clock Sources

A high accuracy crystal with ±10ppm tolerance is connected to the BM77SPP03MC2 clock input pins.

- Serial Flash and Firmware Version

Firmware code is stored on chip internal flash.

- Radio Characteristics

Frequency Band: 2402-2480 GHz

Number of Channels:

Bluetooth V3.0 + EDR	Low Energy
79 channels (1MHz)	40 MHz channels (2MHz)

- Current Consumption (It is the average current consumption and measured by FLUKE multi-meter)

Class BR/ EDR (UART RX_IND Function Enable)

Operation Mode	Peak current	AVG current	Unit	Note
Peak current at TX mode	48.82		mA	
Peak current at RX mode	44.76		mA	
Deep power down mode		0.37	mA	
Connected + Sniff, Master (No data)		2.26	mA	No data was transmitted Sniff (40 20 4 0)
Connected + Sniff, Master (No data)		0.84	mA	No data was transmitted Sniff (500 20 4 0)
Connected + Sniff, Slave (No data)		0.82	mA	No data was transmitted Sniff (500 20 3 3) iPhone parameters
Data, Master		17.35	mA	Data transmitted at 115200bps
Data, Slave		20.04	mA	Data transmitted at 115200bps

Low Energy (UART RX_IND Function Enable)

Operation Mode	AVG current	Unit	Note
Standby mode (Advertising)	4.89	mA	Adv interval = 20ms
	0.97	mA	Adv interval = 160ms
	0.86	mA	Adv interval = 1000ms
Deep power down mode	0.102	mA	
Connected	2.76	mA	Connection interval = 20ms
	0.84	mA	Connection interval = 500ms
	0.81	mA	Connection interval = 1000ms
Connected with data transmit (20 bytes MCU data/Connection Event)	6.16	mA	Connection interval = 20ms
	1.12	mA	Connection interval = 500ms
	0.94	mA	Connection interval = 1000ms

- Terminal characteristics

Condition : VDD_IO=3.3V	**Min**	**Typ**	**Max**	**Unit**
I/O voltage levels				
V_{IL} input logic levels low	-0.3		0.8	V
V_{IH} input logic levels high	2.0		3.6	V
V_{OL} output logic levels low			0.4	V
V_{OH} output logic levels high	2.4			V
Reset terminal				
$V_{TH,res}$ threshold voltage		1.6		V
Input and tri-state current with				
Pull-up Resistor		65		Kohm
Leakage current	-10		+10	μA
Vdd supply current				
TX mode			70	mA
RX mode			70	mA

- Baud Rate

Desired baud rate	Clock	Actual Baud rate	Error Rate %
921600	16000000	941176	-2.12
460800	16000000	457143	0.79
307200	16000000	307692	-0.16
230400	16000000	231884	-0.64
115200	16000000	111888	-2.87
57600	16000000	58608	1.75
38400	16000000	38462	0.16
28800	16000000	28623	-0.62
19200	16000000	19231	0.16
14400	16000000	14480	0.55
9600	16000000	9615	0.16
4800	16000000	4808	0.16
2400	16000000	2399	-0.03

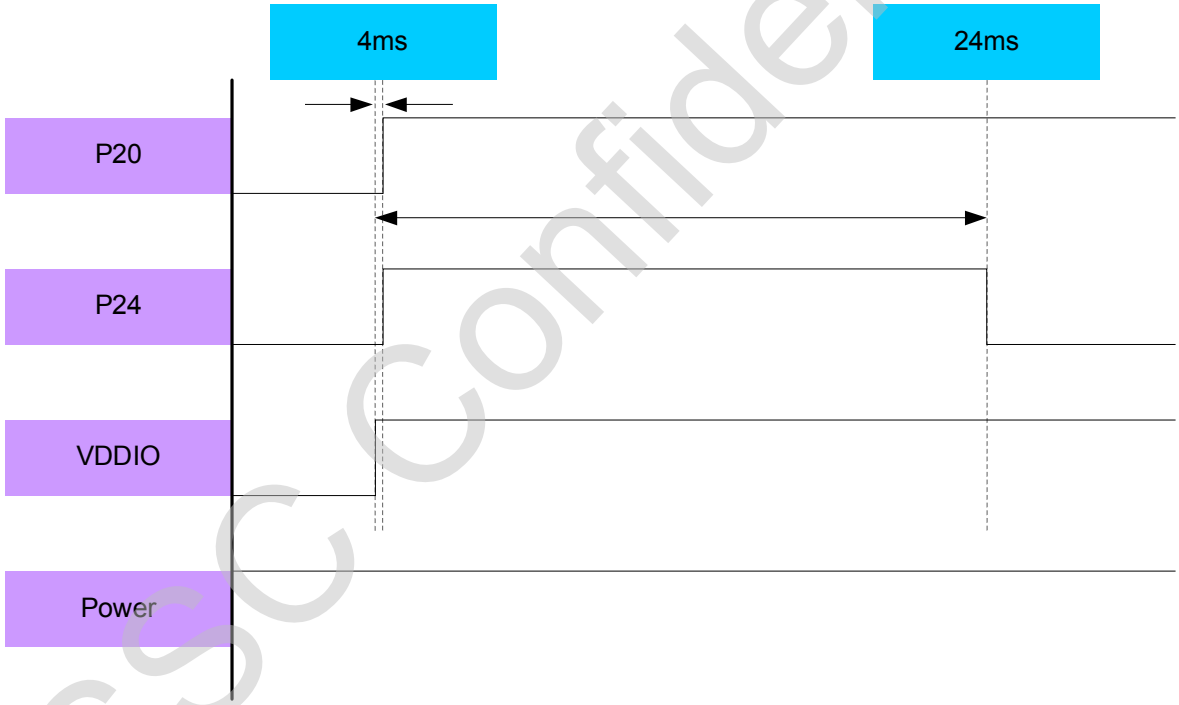
- Testing Criterion

NO.	Testing Item Name	Spec.
1	Device Initialization	
2	System Verify	System Power>1.6V
3	PMU LDO trim	1.8~2.1
4	Calibration LDO18	1.85~1.97V
5	Calibration LDO33	3.1~3.4V
6	RF frequency calibration	< 10k Hz
7	RF TX power verify	> -5 dBm
8	8852 output power	-2dbm~+4dbm
9	Initial carrier test	+/- 30KHz
10	Single slot sensitivity	> -70dbm
11	Multi slot sensitivity	> -70dbm
12	Modulation index test	‘140KHz ≦ f1avg ≦ 175KHz f2max ≧ 115KHz f2/f1avg ≧ 0.8

- Timing Sequence

Timing Sequence for Mode selection Pin (P20, P24) under APP mode

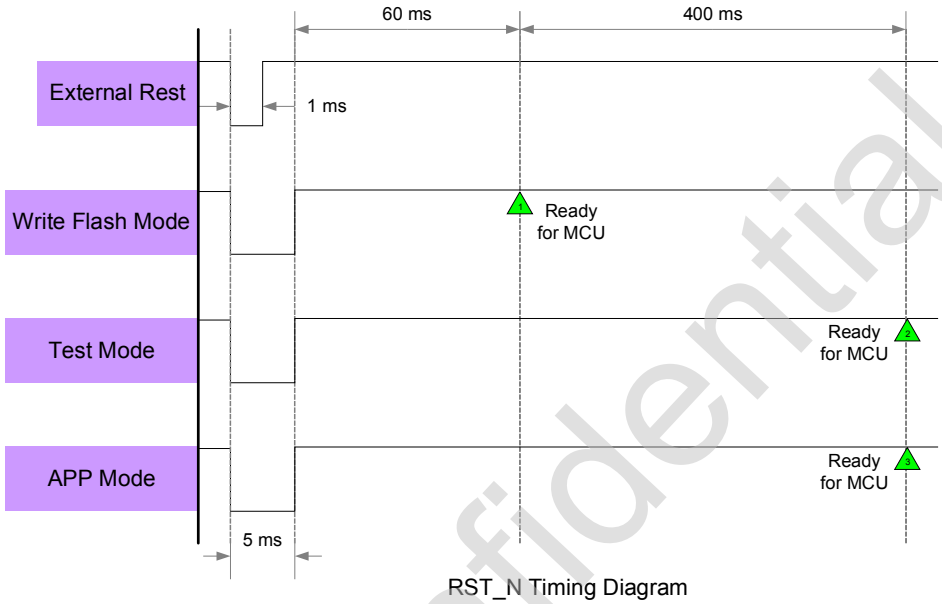
Pin No.	I/O	Name	Description
4	I	BAT_IN	4.2V~3.2V power input
7	P	VDD_IO	Main power supply
17	I	P20	System configuration, refer to P2_4, MCU do **NOT drive under APP Mode**
18	I	P24	Boot mode selection (MCU **NOT drive under APP Mode**) P2_0/ P2_4: HH → Application LL → Boot mode LH → HCI UART mode for testing and system configuration.



P20, P24 Mode Selection Timing Diagram

Timing Sequence for Rest Pin (RST_N) under different mode

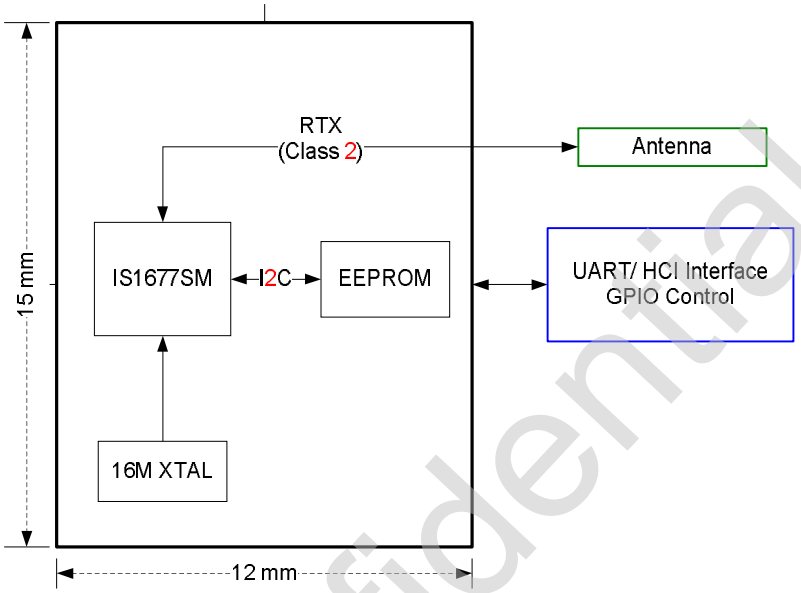
22	I	**RST_N**	**External reset input (Low Active), clock period 62.5n at least.**



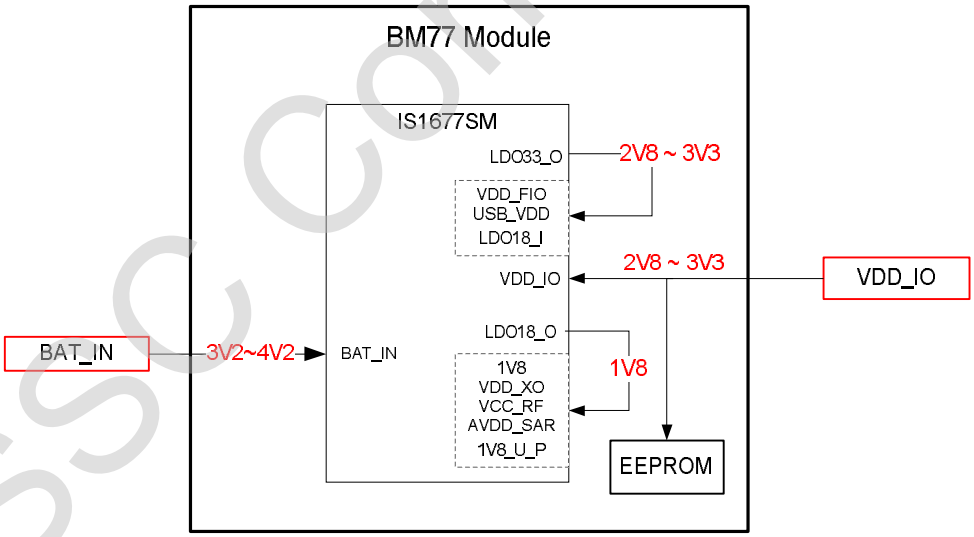
RST_N Timing Diagram

3. Hardware Architecture

Block Diagram



Power Tree



4. Compatibility Requirements

The BM77SPP03MC2 Bluetooth module shall pass the standard test plan, which includes hardware compatibility and reliability, and software compatibility test.

5. Environmental Requirements

5.1. Temperature

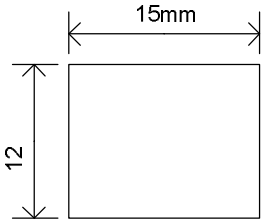
Conditions	Operating Temperature	Non-Operating Temperature
Minimum	-10 ℃	-40℃
Maximum	+70 ℃	+85 ℃

5.2. Humidity

Conditions	Operating Humidity	Non-Operating Humidity
Minimum	10%	5%
Maximum	90%	95%

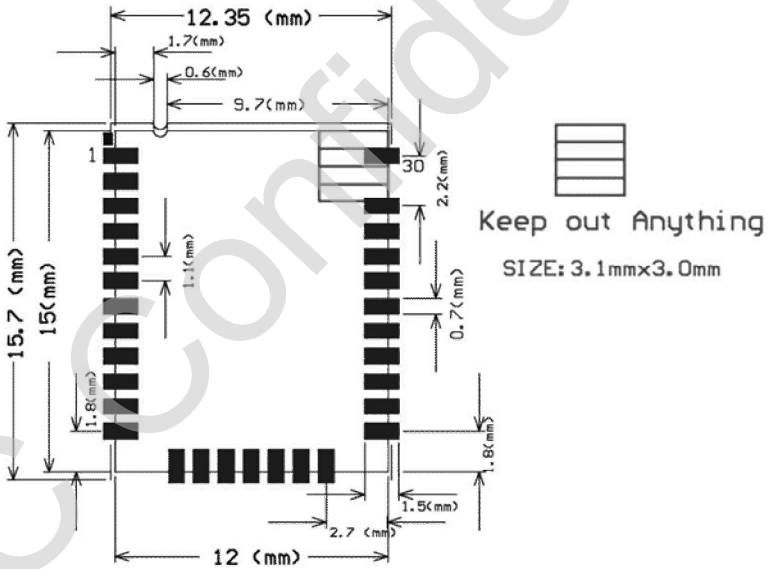
Appendix A: Dimension and Foot Print

1. Dimension



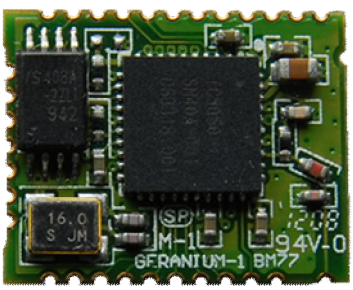
- Dimension: 15 mm* 12 mm* 1.86 mm (Length* Width* Height)
- Tolerance: +/- 0.25 mm

2. Suggested Load Board Foot Print



module size:15mmx12mm
screen outline:15.7mmx12mm
pad size:1.5mmx0.7mm
pad pitch:1.27mm

Appendix B: Product Image



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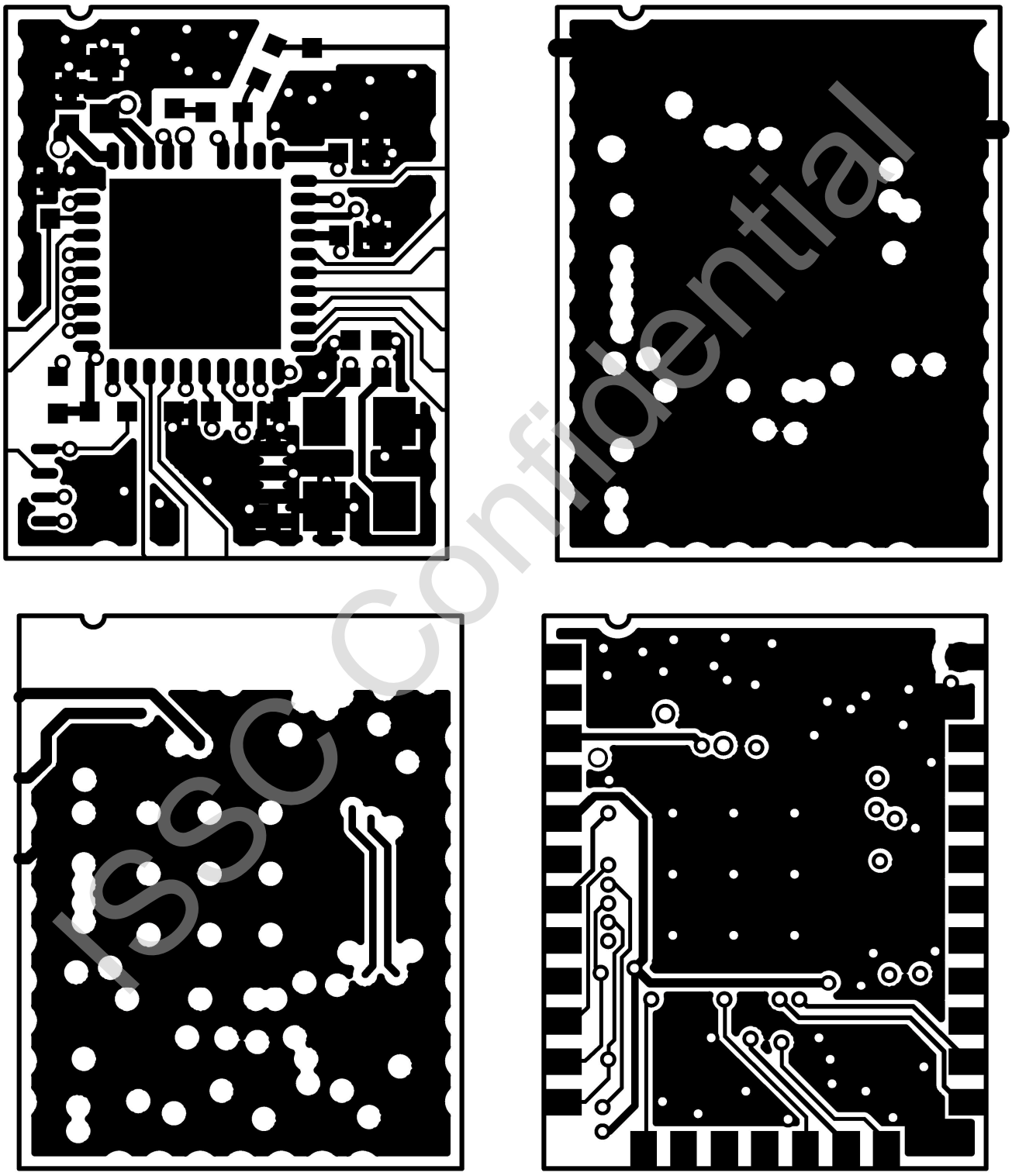
Appendix C: Geber



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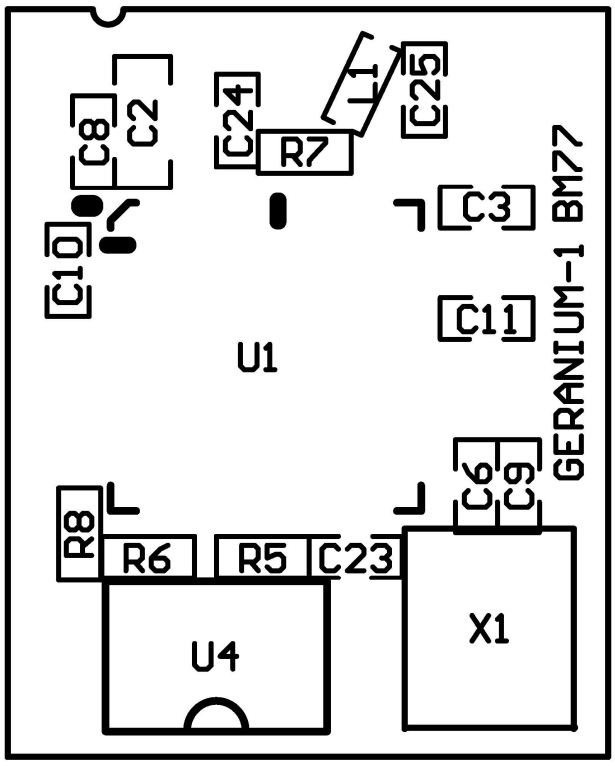
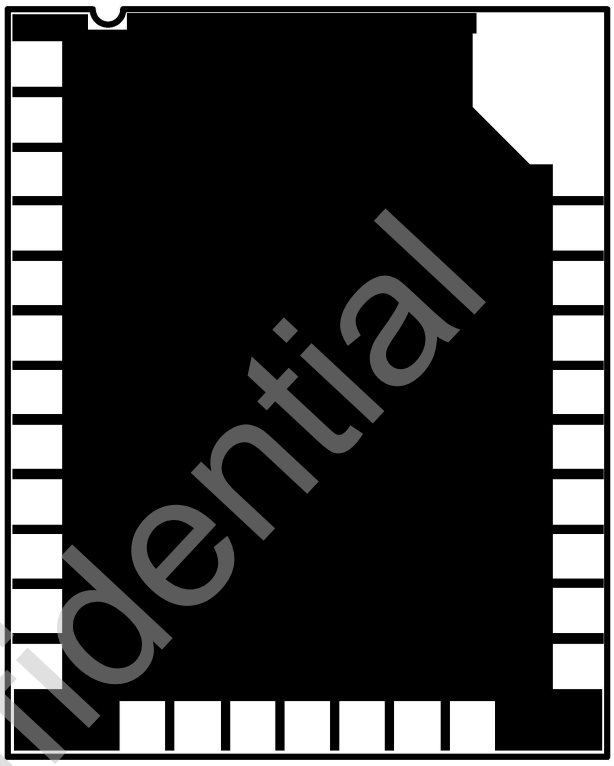
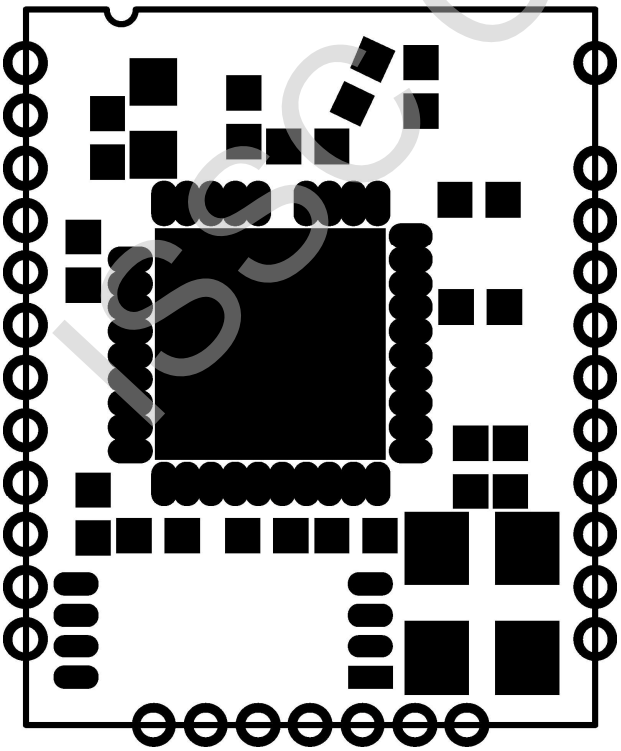
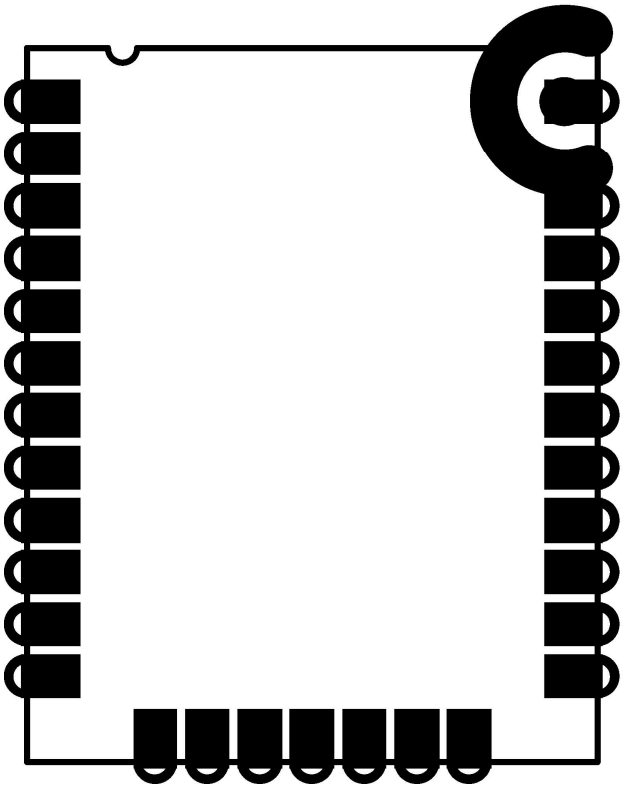
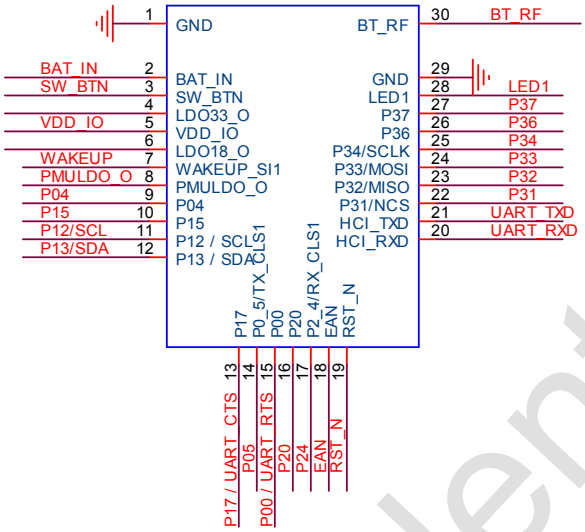








Appendix D: PIN Assignment



P/N	I/O	Name	Description
1	P	GND	Ground
2	P	BAT_IN	4.2~3.2V Power input
3	I	SW_BTN	Input for software button. H: Power On L: Power Off
4	P	LDO33_O	3V3 LDO output
5	P	VDD_IO	Main power supply
6	P	LDO18_O	LDO18 output
7	I	WAKEUP	Wakeup BM77 from Shutdown State. (Low Active) It is only valid while BM77 into Shutdown State.
8	P	PMULDO_O	Output of PMULDO
9	O	P04	UART_TX_IND: H: BM77 indicate UART data will be transmitted out after a certain timing. (Setting by EEPROM, default 5ms) L: Otherwise. STATUS_IND_2: BM77 State indication , refer to P15

P/N	I/O	Name	Description
10	O	P15	STATUS_IND: Bluetooth link status indication P15/P04: HH → Power default value and Shutdown State. P15/P04: HL → Access State. P15/P04: LL → Link State w/o UART_TXD. P15/P04: LH → Link State with UART_TXD.
11	N/A	P12/ SCL	Reserved
12	N/A	P13/ SDA	Reserved
13	I	**P17**	- UART_CTS: - Configurable Functional GPIO
14	I/O	**P05**	Configurable Functional GPIO
15	O	**P00**	- UART_RTS - Configurable Functional GPIO
16	I	P20	System configuration, refer to P2_4. (No drive under APP Mode)
17	I	P24	Boot mode selection. (No drive under APP Mode) P2_0/ P2_4: HH → Application LL → Boot mode LH → HCI UART mode for testing and system configuration.
18	I	EAN	ROM/Flash selection. (No drive under APP Mode) H: ROM code; L: Flash code
19	I	RST_N	External reset input (Low Active), Clock period 62.5n at least
20	I	HCI_RXD	UART_RXD
21	O	HCI_TXD	UART_TXD
22	I/O	**P31**	Configurable Functional GPIO
23	I	**P32**	Configurable Functional GPIO
24	I	**P33**	Configurable Functional GPIO
25	I	**P34**	Configurable Functional GPIO
26	O	P36	Reserved
27	I/O	**P37**	Configurable Functional GPIO
28	O	LED1	LED1 driver
29	P	GND	Ground
30	RI/O	BT_RF	RF Port

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Appendix E: Reflow Profile

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.

Preheat：150~200C、60~180 seconds

Temperature maintained above 217℃ : 60~150 seconds

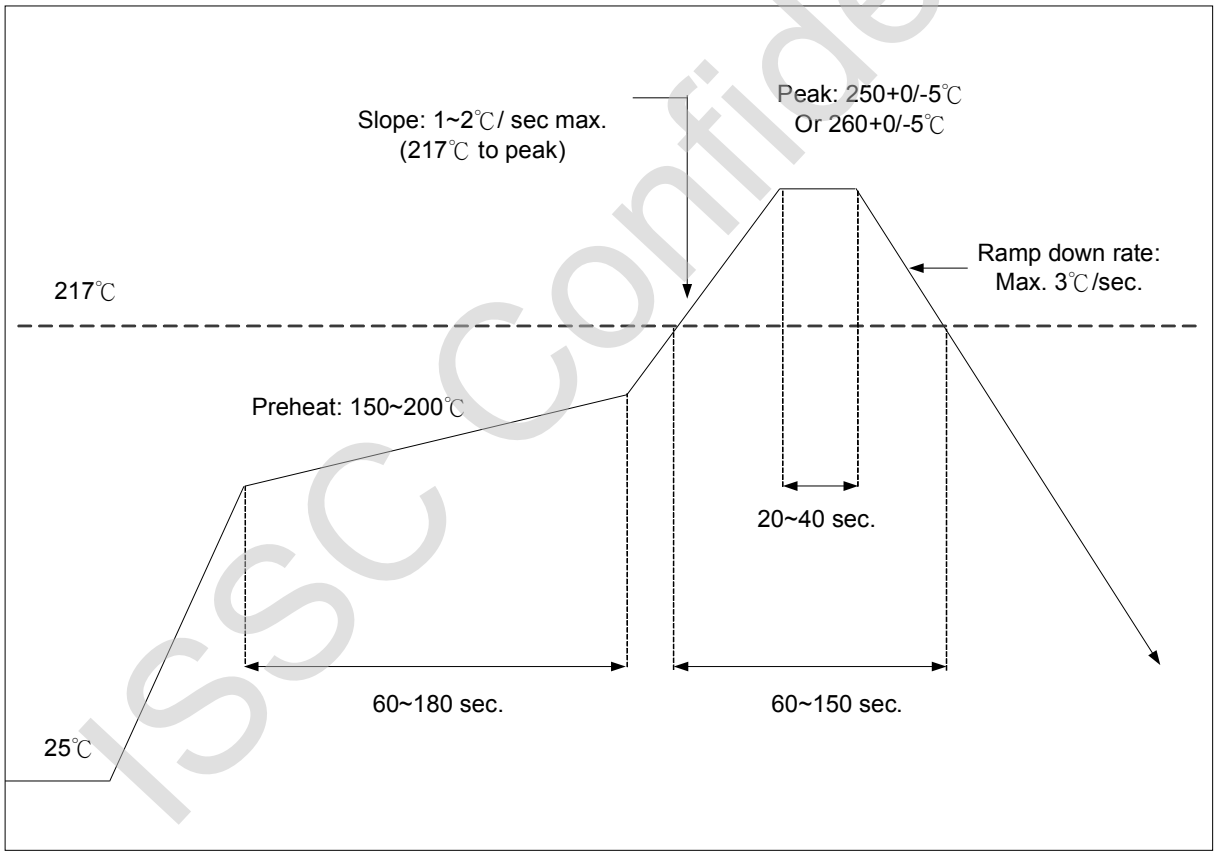
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.

Peak temperature：250+0/-5℃ or 260+0/-5℃

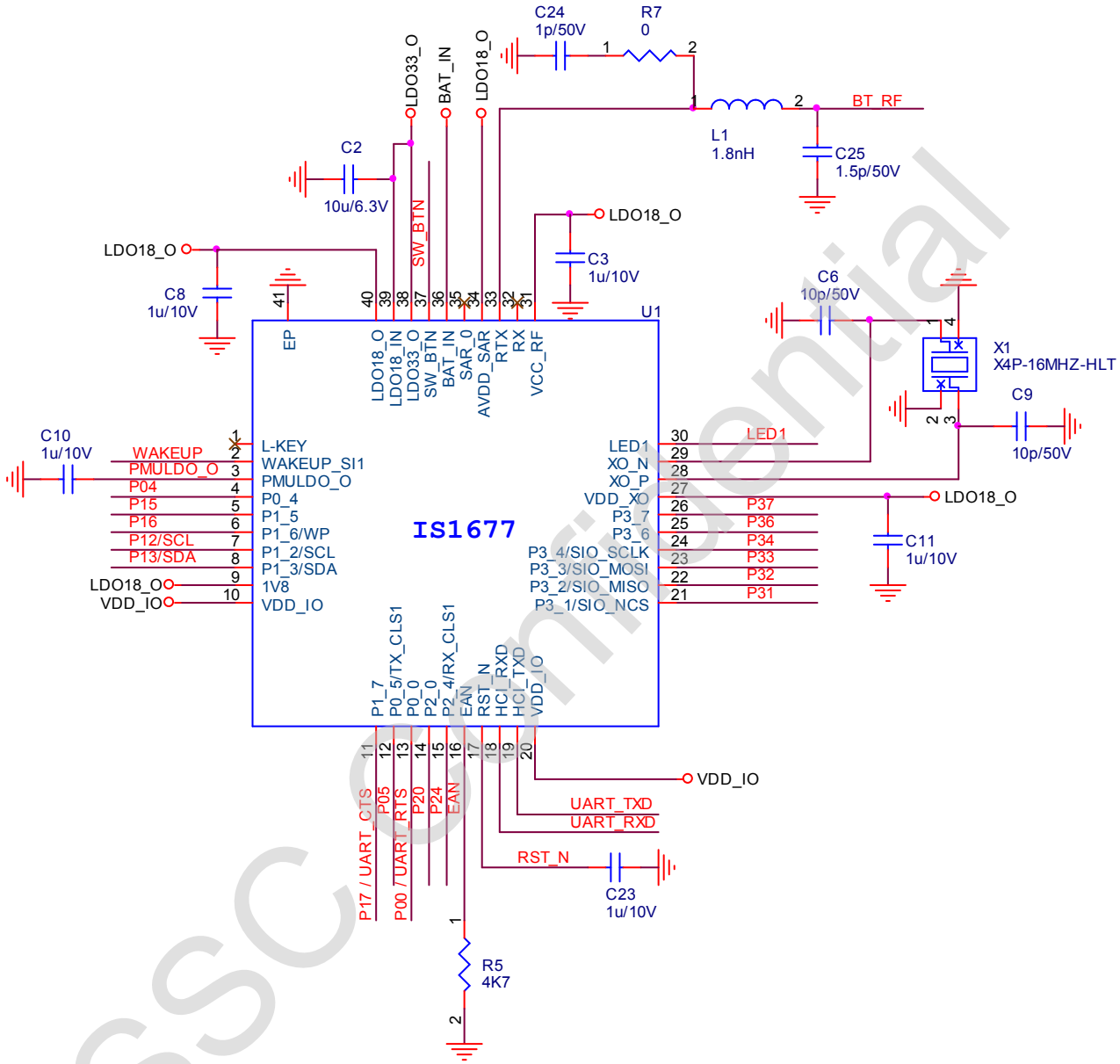
Ramp-down rate : 3℃/sec. max.

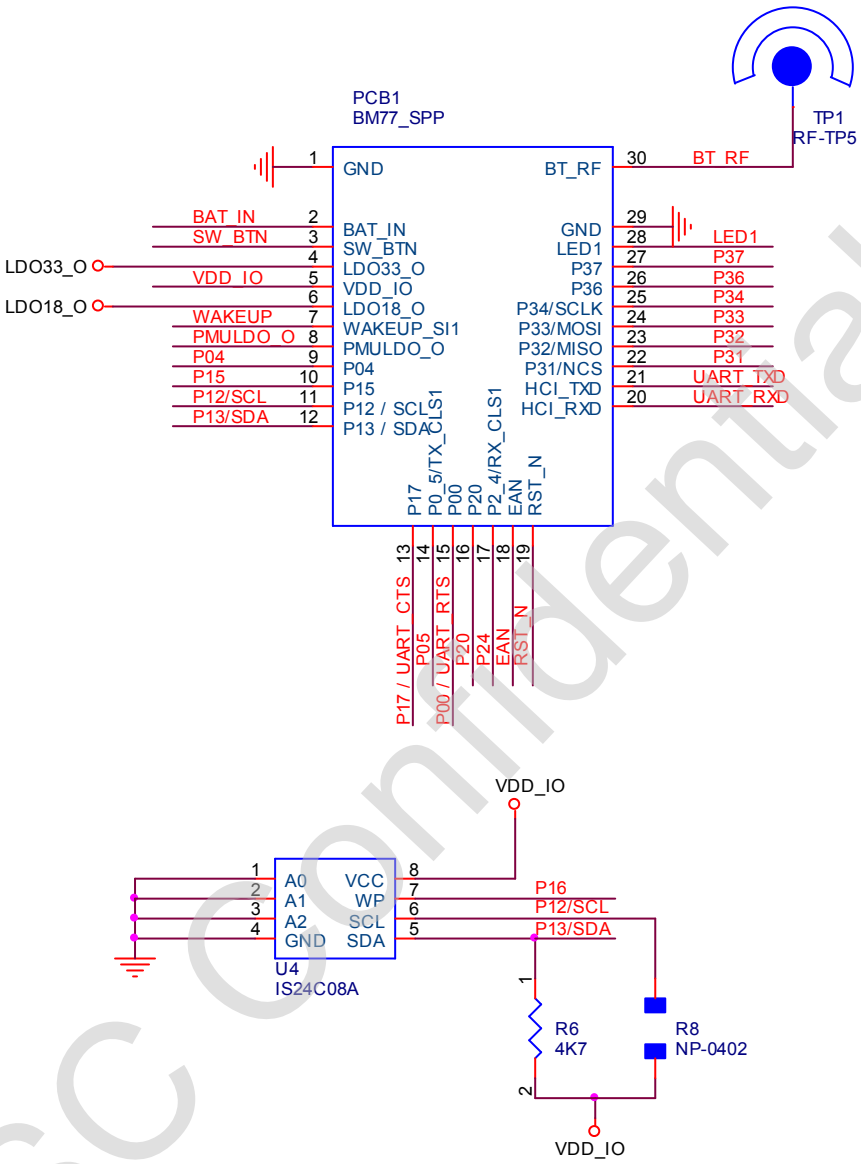
Time 25℃ to peak temperature : 8 minutes max.

Cycle interval：5 minus

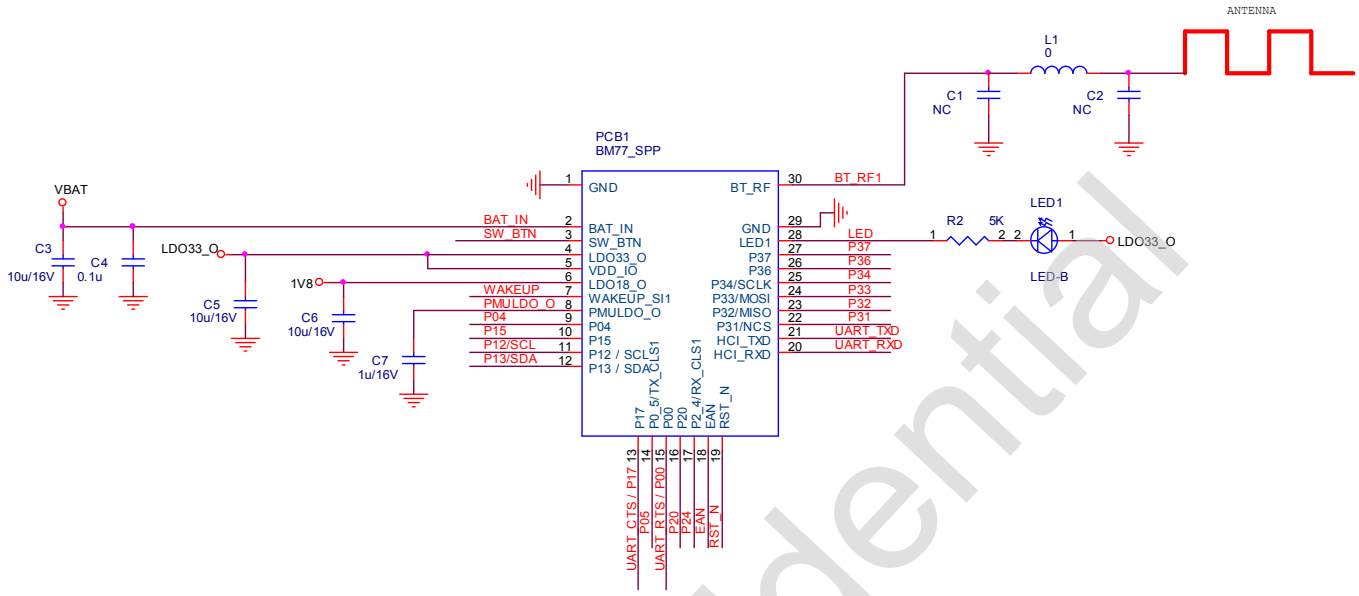


Appendix F: Schematic





Appendix G: Reference Schematic



EAN, P20, P24 are recommended to reserve with test point for future firmware, EEPROM table update after the module are welded on load board.

Appendix H: Label Information

TBA

Appendix I: Packaging Information

TBA

Appendix J: Reversion History

Version	Date	History
0.2	2012/8/23	Modified support baud rate
0.3	2012/10/31	Modified the Calibration values of LDO18 Fixed for module schematic
0.4	2013/01/30	Modified Figure Error in page_15
1.3	2013/08/20	Update UART Baud rate information
1.4	2013/10/01	Update current consumption & Timing Sequence photo